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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
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| 09/122,349 | 07/24/98 | HACKING | L 042390.P5965 |

| EXAMINER | |
|---|---|
| TRAN, D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | 6 |

TM02/0314
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES CA 90025

**DATE MAILED:** 03/14/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

RE

PTO-90C (Rev. 2/95)
1- File Copy
*U.S. GPO: 2000-473-000/44602

| Office Action Summary | Application No | Applicant(s) | |
|---|---|---|---|
| | 09/122,349 | HACKING ET AL. | |
| | Examiner | Art Unit | |
| | Denise Tran | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

**Status**

1)☒ Responsive to communication(s) filed on *20 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

14) ☒ Notice of References Cited (PTO-892)
15) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

## DETAILED ACTION

1. In response to the applicant's requests during the telecommunication on 03/08/01, claims 13-37 have been rejoined, the restriction requirement made in Paper No. 3 is hereby withdrawn.

2. Claims 1-37 are presented for examination.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rahman et al., U.S. patent No. 5,778,431, (hereinafter Rahman).

As per claims 1, 7, 13, 18, 24, 29 and 35-36, Rahman teaches the invention substantially as claimed, comprising: a first storage area to store data (e.g., fig. 1, el. 114); a cache memory having a plurality of cache lines, each of which stores data (e.g., fig.1, el. 106 and col. 5, line 27 and et seq.); a second storage area to store instructions (e.g., col. 7, line 22 and et seq.); and an execution unit coupled to the first storage area, the second storage area, and the cache memory to operate on data elements to invalidate data in a predetermined portion of the plurality of cache lines in response to receiving an instruction (e.g., col. 7, line 22 and et seq.) or copy data in a

predetermined portion of the plurality of cache lines to the first storage area in response to receiving an instruction (e.g., col. 7, line 22 and et seq.); or a processor comprising a circuit to obtain a starting address of a predetermined area of the cache memory (e.g., fig.1, els. 101 or 102) and invalidate data in the predetermined area of cache memory (e.g., col. 7, line 22 and et seq.) or copy data from the predetermined are of cache memory and store the copy data in the storage area separate from the cache memory (e.g., col. 7, line 22 and et seq.). Even though Rahman teaches the use of validation being implemented through instruction and operating address values to invalidate or copy data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand. "Official Notice" is taken that both the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would instruct the system to do work by using data it its operand and thereby, increase controlling of the system. Rahman does not specifically show the use of decoder to decode instructions. "Official Notice" is taken that both the concept and advantages of providing a decoder to decode an instruction are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction.

As per claims 2-4, 6, 8-9, 11-12, 14-15, 17, 19-20, 22-23, 25, 28, 30, 33-34, and 37, Rahman shows a register address values (i.e., a memory register address; e.g., col.7); a portion of a starting address of the cache line in which data to be invalidated or copied (i.e., tag address; e.g., col. 7, line 22 and et seq.); the portion of a starting address including a plurality of most significant bits of the starting address (i.e., tag address; e.g., col. 7, line 22 and et seq.); the predetermined portion of the plurality of cache lines is a page in the cache memory (i.e., a page can be a cache line; e.g., col.7); an execution unit coupled to the first storage area, the second storage area, and the cache memory to operate on data elements to invalidate data in a predetermined portion of the plurality of cache lines in response to receiving an instruction (e.g., col. 7, line 22 and et seq.) or copy data in a predetermined portion of the plurality of cache lines to the first storage area in response to receiving an instruction (e.g., col. 7, line 22 and et seq.); and setting an invalid bit corresponding to the predetermined area of cache memory (e.g., col. 5, line 40 and et seq.) . Even though Rahman teaches the use of validation being implemented through instruction and operating address values to invalidate or copy data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand. "Official Notice" is taken that both the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would instruct the system to do work by using data it its operand

and thereby, increase controlling of the system. Rahman does not specifically show the use of decoder to decode instructions. "Official Notice" is taken that both the concept and advantages of providing a decoder to decode an instruction are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction.

As per claims 5, 10, 16, 21, 26-27, 31-32, Rahman shows the portion of a starting address including a plurality of most significant bits of the starting address (i.e., tag address; e.g., col. 7, line 22 and et seq.); Rahman does not specifically show execution unit shifts the data elements by a predetermined number of bits positions represent a number of least significant bits to obtain the starting address of the cache line in which data to be invalidated or copied. Even though Rahman teaches the use of validation being implemented through instruction and operating address values to invalidate or copy data (e.g., col. 7, line 22 and et seq.) but does not specifically show the use of providing a single instruction with an operand. "Official Notice" is taken that both the concept and advantages of providing a single instruction with an operation code and address values in its operand are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a single instruction with an operation code and address values in its operand to Rahman's system because it would instruct the system to do work by using data it its operand and thereby, increase controlling of the system. Rahman does not specifically show the use of decoder to decode

instructions. "Official Notice" is taken that both the concept and advantages of providing a decoder to decode an instruction are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a decoder to Rahman's system because it would produce an operation and a address values of an instruction. "Official Notice" is taken that both the concept and advantages of shifting the data elements by a predetermined number of bits positions are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have shifting the data elements by a predetermined number of bits positions to Rahman's system because it would allow rearrange an order of address bits in a particular sequence.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday and Thursday from 7.30 p.m. to 6.00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone number for this Group is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

D.T.

Denise Tran

03/9/01

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100